

CLAIMS:

1. A board on chip package, comprising:
an insulative substrate having circuitry thereon and an opening therethrough;
a semiconductive-material-comprising die adhered to the substrate and electrically connected to the circuitry with a plurality of electrical interconnects extending through the opening; and
a metal foil in physical contact with at least a portion of the die.
2. The board on chip package of claim 1 wherein the foil is adhered to the substrate with an electrically conductive epoxy.
3. The board on chip package of claim 1 wherein the die has a first surface facing the substrate and a second surface in opposing relation to the first surface, the foil being in physical contact with only a portion of said second surface.
4. The board on chip package of claim 1 wherein the die has a first surface facing the substrate and a second surface in opposing relation to the first surface, the foil being in physical contact with an entirety of said second surface.

1 5. The board on chip package of claim 1, wherein the die has
2 a first surface facing the substrate, a second surface in opposing relation
3 to the first surface, and a sidewall between the first and second surfaces,
4 the foil being adhered to the substrate proximate the sidewall and
5 extending across the sidewall to physically contact the second surface.
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7 6. The board on chip package of claim 5 wherein the sidewall
8 has a length, and wherein the foil physically contacts a predominate
9 portion of the sidewall length.
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11 7. The board on chip package of claim 5 wherein the sidewall
12 has a length, and wherein the foil is spaced from a predominate portion
13 of the sidewall length by a gap.
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15 8. The board on chip package of claim 5 wherein the sidewall
16 has a length, wherein the foil is spaced from a predominate portion of
17 the sidewall length by a gap, and wherein the gap has electrically
18 conductive epoxy extending from the sidewall to the foil.
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1 9. The board on chip package of claim 5 wherein the sidewall
2 has a length, wherein the foil is spaced from a predominate portion of
3 the sidewall length by a gap, and wherein the gap is filled with
4 electrically conductive epoxy extending from the sidewall to the foil.
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6 10. The board on chip package of claim 1 wherein the metal foil
7 is selected from the group consisting of copper foil and aluminum foil.
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9 11. The board on chip package of claim 1 wherein the die is
10 adhered to the substrate with an electrically conductive epoxy.
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12 12. A board on chip package, comprising:
13 an insulative substrate having circuitry thereon and an opening
14 therethrough;

15 a semiconductive-material-comprising die adhered to the substrate
16 and electrically connected to the circuitry with a plurality of electrical
17 interconnects extending through the opening; and

18 a metal foil adhered to a portion of the die with an electrically
19 conductive adhesive.
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1 13. The board on chip package of claim 12 wherein the die has
2 a first surface facing the substrate and a second surface in opposing
3 relation to the first surface, the foil being in physical contact with only
4 a portion of said second surface.

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6 14. The board on chip package of claim 12 wherein the die has
7 a first surface facing the substrate and a second surface in opposing
8 relation to the first surface, the foil being in physical contact with an
9 entirety of said second surface.

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11 15. The board on chip package of claim 12 wherein the die has
12 a first surface facing the substrate, a second surface in opposing relation
13 to the first surface, and a sidewall between the first and second surfaces,
14 the foil being adhered to the substrate proximate the sidewall and
15 extending across the sidewall to physically contact the second surface.

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17 16. The board on chip package of claim 15 wherein the sidewall
18 has a length, and wherein the foil physically contacts a predominate
19 portion of the sidewall length.
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1 17. The board on chip package of claim 15 wherein the sidewall
2 has a length, and wherein the foil is spaced from a predominate portion
3 of the sidewall length by a gap.

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5 18. The board on chip package of claim 15 wherein the sidewall
6 has a length, wherein the foil is spaced from a predominate portion of
7 the sidewall length by a gap, and wherein the gap has electrically
8 conductive epoxy extending from the sidewall to the foil.

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10 19. The board on chip package of claim 15 wherein the sidewall
11 has a length, wherein the foil is spaced from a predominate portion of
12 the sidewall length by a gap, and wherein the gap is filled with
13 electrically conductive epoxy extending from the sidewall to the foil.

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15 20. The board on chip package of claim 12 wherein the metal
16 foil is selected from the group consisting of copper foil and aluminum
17 foil.

1 21. A board on chip package, comprising:
2 an insulative substrate having circuitry thereon and an opening
3 therethrough;

4 a semiconductive-material-comprising die adhered to the substrate
5 and electrically connected to the circuitry with a plurality of electrical
6 interconnects extending through the opening, the die having a first
7 surface facing the substrate, a second surface in opposing relation to the
8 first surface, and a sidewall surface extending between the first and
9 second surfaces; and

10 a thermally conductive material in physical contact with at least
11 two of the die first surface, second surface and sidewall surface; the
12 thermally conductive material having a thermal conductivity under
13 specified conditions equal to or greater than the thermal conductivity of
14 elemental copper under the same specified conditions.

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16 22. The board on chip package of claim 21 wherein the
17 thermally conductive material comprises a silver-filled epoxy.

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19 23. The board on chip package of claim 21 wherein the
20 thermally conductive material comprises a metal foil.
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1 24. The board on chip package of claim 21 wherein the
2 thermally conductive material comprises a material selected from the
3 group consisting of aluminum foil and copper foil.
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5 25. The board on chip package of claim 21 wherein the
6 thermally conductive material is in physical contact with the second
7 surface.
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9 26. The board on chip package of claim 21 wherein the
10 thermally conductive material is in physical contact with the sidewall and
11 the second surface.
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13 27. The board on chip package of claim 21 wherein the
14 thermally conductive material is in physical contact with the sidewall, the
15 first surface and the second surface.
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1 28. A board on chip package, comprising:

2 an insulative substrate having circuitry thereon and an opening
3 therethrough, the substrate comprising a first surface and a second
4 surface in opposing relation to the first surface, the circuitry being on
5 the first surface, the substrate further comprising a cavity extending into
6 the second surface and proximate the opening;

7 a semiconductive-material-comprising die received within the cavity
8 and electrically connected to the circuitry with a plurality of conductive
9 interconnects extending through the opening, the die having an inner
10 surface facing the substrate and an outer surface in opposing relation to
11 the inner surface; and

12 a metal sheet in physical contact with at least a portion of the die
13 outer surface.

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15 29. The board on chip package of claim 28 wherein the die is
16 entirely received in the cavity inwardly of the second surface of the
17 substrate, and wherein the sheet extends along the second surface of the
18 substrate and over the cavity to enclose the die in the cavity.

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20 30. The board on chip package of claim 28 wherein the metal
21 sheet is selected from the group consisting of copper foil and aluminum
22 foil.
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1 31. The board on chip package of claim 28 wherein the die is
2 adhered to the substrate with an electrically conductive epoxy.
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1 32. A board on chip package, comprising:
2 an insulative substrate having a pair of opposing surfaces and an
3 opening extending therethrough, the opposing surfaces being a first
4 surface and a second surface;
5 circuitry on the first surface of the substrate;
6 a semiconductive-material-comprising die adhered to the second
7 surface of the substrate, the die having a pair of opposing surfaces, one
8 of the die opposing surfaces being a first die surface and being aligned
9 to face toward the second surface of the substrate, the other die surface
10 being a second die surface and being aligned to face away from the
11 second surface of the substrate, the die further comprising first and
12 second opposing sidewalls extending between the first and second
13 surfaces;
14 electrical interconnects extending from the die, through the opening
15 and to the circuitry;
16 a metal foil contacting the substrate at a first location proximate
17 the first sidewall and a second location proximate the second sidewall,
18 the metal foil extending across the first and second sidewalls and over
19 the second die surface; the metal foil physically contacting a predominate
20 portion of the second die surface.
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1 33. The board on chip package of claim 32 wherein the metal
2 foil comprises a foil selected from the group consisting of aluminum foil
3 and copper foil.
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5 34. The board on chip package of claim 32 wherein the foil is
6 adhered to the substrate with an electrically conductive epoxy.
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8 35. The board on chip package of claim 32 wherein the foil is
9 in physical contact with only a portion of the second die surface.
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11 36. The board on chip package of claim 32 wherein the foil is
12 in physical contact with an entirety of the second die surface.
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14 37. The board on chip package of claim 32 wherein the sidewall
15 has a length, and wherein the foil physically contacts a predominate
16 portion of the sidewall length.
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18 38. The board on chip package of claim 32 wherein the sidewall
19 has a length, and wherein the foil is spaced from a predominate portion
20 of the sidewall length by a gap.
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1 39. The board on chip package of claim 32 wherein the sidewall
2 has a length, wherein the foil is spaced from a predominate portion of
3 the sidewall length by a gap, and wherein the gap has electrically
4 conductive epoxy extending from the sidewall to the foil.

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6 40. The board on chip package of claim 32 wherein the die is
7 adhered to the substrate with an electrically conductive epoxy.

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9 41. The board on chip package of claim 32 wherein the die
10 comprises a rectangular outer periphery having four sides, wherein the
11 metal foil extends outwardly beyond the outer periphery of the die and
12 contacts the substrate at locations proximate each of the four sides.

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14 42. A method of forming a board on chip package, comprising:
15 providing an insulative substrate having circuitry thereon and an
16 opening therethrough;

17 adhering a semiconductive-material-comprising die to the substrate
18 with an electrically conductive adhesive, the die having circuitry supported
19 thereby; and

20 electrically connecting the circuitry supported by the die to the
21 circuitry on the substrate with a plurality of electrical interconnects
22 extending through the opening.
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1 43. The method of claim 42 wherein the electrically conductive
2 adhesive comprises silver-filled epoxy.

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4 44. The method of claim 42 wherein the die has a surface, and
5 further comprising placing a metal foil in physical contact with at least
6 a portion of the die surface.

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8 45. A method of forming a board on chip package, comprising:
9 providing an insulative substrate having circuitry thereon and an
10 opening therethrough;

11 adhering a semiconductive-material-comprising die to the substrate
12 and electrically connecting circuitry supported by the die with the
13 circuitry on the substrate utilizing a plurality of electrical interconnects
14 extending through the opening; and

15 joining a metal foil to the substrate, the metal foil having a
16 segment extending over the die and in physical contact with at least a
17 portion of the die.

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19 46. The method of claim 45 wherein the joining the metal foil
20 to the substrate comprises welding the metal foil to the substrate by
21 melting a portion of the metal foil with a portion of the substrate.
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1 47. The method of claim 46 wherein the melting is accomplished
2 with a laser.

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4 48. The method of claim 45 wherein the joining the metal foil
5 to the substrate comprises adhering the metal foil to the substrate with
6 an electrically conductive epoxy.

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8 49. The method of claim 45 wherein the die has a first surface
9 facing the substrate and a second surface in opposing relation to the
10 first surface, the foil being in physical contact with only a portion of
11 said second surface.

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13 50. The method of claim 45 wherein the die has a first surface
14 facing the substrate and a second surface in opposing relation to the
15 first surface, the foil being in physical contact with an entirety of said
16 second surface.

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18 51. The method of claim 45 wherein the die has a first surface
19 facing the substrate, a second surface in opposing relation to the first
20 surface, and a sidewall between the first and second surfaces, the foil
21 being joined to the substrate proximate the sidewall and extending across
22 the sidewall to physically contact the second surface.
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1 52. The method of claim 51 wherein the sidewall has a length,
2 and wherein the foil physically contacts a predominate portion of the
3 sidewall length.
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5 53. The method of claim 51 wherein the sidewall has a length,
6 and wherein the foil is spaced from a predominate portion of the
7 sidewall length by a gap.
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9 54. The method of claim 51 wherein the sidewall has a length,
10 wherein the foil is spaced from a predominate portion of the sidewall
11 length by a gap, and wherein the gap has electrically conductive epoxy
12 extending from the sidewall to the foil.
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14 55. The method of claim 45 wherein the metal foil is selected
15 from the group consisting of copper foil and aluminum foil.
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17 56. The method of claim 45 further comprising adhering the die
18 to the substrate with an electrically conductive epoxy.
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1 57. A method of forming a board on chip package, comprising:
2 providing an insulative substrate having circuitry thereon and an
3 opening therethrough, the substrate having a pair of opposing surfaces,
4 the surfaces being a first surface and a second surface, the circuitry
5 being on the first surface;

6 adhering a metal foil to the second surface;

7 adhering a semiconductive-material-comprising die to the metal foil,
8 the die having circuitry supported thereby; and

9 electrically connecting the circuitry supported by the die to the
10 circuitry on the substrate with a plurality of electrical interconnects
11 extending through the opening.
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13 58. The method of claim 57 wherein the die has a pair of
14 opposing sides; wherein the die covers a portion of the metal foil and
15 leaves an other portion of the metal foil extending outwardly beyond one
16 of the opposing sides of the die; and further comprising wrapping at
17 least some of said other portion of the foil along the at least one of
18 the opposing sides of the die.
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1 59. The method of claim 58 wherein the die comprises a first
2 surface facing the substrate and second surface in opposed relation to
3 the first surface, the other portion of the foil being wrapped along both
4 of the opposing sides of the die and over the second surface of the die.
5

6 60. The method of claim 57 wherein the die has a pair of
7 opposing sides; wherein the die covers a portion of the metal foil and
8 leaves a pair of other portions of the metal foil extending outwardly
9 beyond the opposing sides of the die; said pair of other portions
10 comprising a first other portion which extends outwardly of the first side
11 of the die, and a second other portion which extends outwardly of the
12 second side of the die; the method further comprising wrapping the first
13 other portion of the foil along the first of the opposing sides of the die,
14 and wrapping the second other portion of the foil along the second of
15 the opposing sides of the die.
16

17 61. The method of claim 60 wherein die comprises a first surface
18 facing the substrate and second surface in opposed relation to the first
19 surface, the first and second other portions of the foil joining one
20 another over the second surface of the die.
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1 62. The method of claim 61 wherein the first and second other
2 portions overlap one another over the second surface of the die.

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4 63. A method of forming a board on chip package, comprising:
5 providing an insulative substrate having circuitry thereon and an
6 opening therethrough, the substrate comprising a first surface and a
7 second surface in opposing relation to the first surface, the circuitry
8 being on the first surface, the substrate further comprising a cavity
9 extending into the second surface and proximate the opening;

10 placing a semiconductive-material-comprising die within the cavity
11 and electrically connecting circuitry supported by the die to the circuitry
12 on the substrate first surface with a plurality of conductive interconnects
13 extending through the opening, the die having an inner surface facing
14 the substrate and an outer surface in opposing relation to the inner
15 surface; and

16 placing a metal sheet outwardly of the die and in physical contact
17 with at least a portion of the die outer surface.
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1 64. The method of claim 63 wherein the die has a portion
2 extending outwardly of the cavity, and wherein the sheet extends along
3 the second surface of the substrate and over the portion of the die
4 extending outwardly of the cavity, the method further comprising bonding
5 the sheet to the second surface of the substrate.

6
7 65. The method of claim 63 wherein the die is entirely received
8 in the cavity inwardly of the second surface of the substrate, and
9 wherein the sheet extends along the second surface of the substrate and
10 over the cavity to enclose the die in the cavity, the method further
11 comprising bonding the sheet to the second surface of the substrate.

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13 66. The method of claim 63 wherein the metal sheet is selected
14 from the group consisting of copper foil and aluminum foil.

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16 67. The method of claim 63 further comprising adhering the die
17 to the substrate with an electrically conductive epoxy.
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1 68. A method of forming a plurality of board on chip packages,
2 comprising:

3 providing an insulative substrate having a repeating circuitry pattern
4 thereon and a plurality of openings therethrough, the openings being in
5 one-to-one correspondence with individual of the repeated circuitry
6 patterns;

7 adhering a plurality of semiconductive-material-comprising dies to
8 the substrate and electrically connecting circuitry supported by the dies
9 with the circuitry on the substrate utilizing a plurality of electrical
10 interconnects extending through the openings;

11 joining a metal foil to the substrate and extending the metal foil
12 over the plurality of dies; and

13 cutting the substrate and metal foil to form singulated die packages
14 comprising a single die, a portion of the substrate having a single
15 repeated pattern of the circuitry, and a portion of the metal foil.

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17 69. The method of claim 68 wherein the substrate comprises
18 areas between the die, and wherein the metal foil is bonded to such
19 areas before the cutting of the substrate.
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1 70. The method of claim 69 wherein the bonding comprises
2 welding the metal foil to the substrate by melting a portion of the metal
3 foil and a portion of the substrate.

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5 71. The method of claim 69 wherein the bonding comprises
6 adhering the metal foil to the substrate with an adhesive.

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8 72. The method of claim 69 wherein the bonding comprises
9 adhering the metal foil to the substrate with an electrically conductive
10 adhesive.

11
12 73. The method of claim 69 wherein the bonding comprises
13 adhering the metal foil to the substrate with silver-filled epoxy.

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15 74. The method of claim 68 wherein the substrate comprises
16 areas between the die, and wherein the metal foil is not bonded to said
17 areas until during or after the cutting of the substrate.

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